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Realising Serial Hybrid Energy Storage Systems (sHESS) by implementing Switching Circuits on Battery Cell Level

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Abstract

One approach to influence the current flow through the battery pack is to implement switching circuits. Two switching elements are necessary for each cell-stage to be bypassed or activated. This allows active *load management*. Thus the utilisation of the battery pack can be maximised in every situation. Adaptive control algorithms allow several kinds of operating strategies. Furthermore, *dynamic output voltage* can be generated to serve the best output for the downstream voltage level. A battery pack with an additional connection at its central point allows the generation of sine-shaped output voltages. As consequence of individual load management, different types of batteries or even different kinds of energy storages can be interconnected to built *serial hybrid electrical energy storages*. This novel approach allows precisely tailored battery packs for each application to enhance performance and energy supply.

Keywords: Load Management, BMS (Battery Management System), Lithium Battery, Charge Equalization, DC-AC

1 Introduction

Today's battery systems for larger scale applications like electric vehicles (EVs) normally consist of static networks. Often several cells are clustered to guarantee a decent level of modularity. Nevertheless, because every battery cell participates in every situation, each of them has to contribute equally to satisfy the load requirements of the respective application. Due to variations during fabrication as well as inhomogeneities within the ageing process, battery cells differ from each other [1, 2]. To maximise the utilisation of a battery pack, usually each single battery cell is actively or passively balanced [3, 4]. Another approach would be selective *load management* using switching elements to activate or inactivate each battery cell individually [5–14]. As shown in fig. 1, two switching circuits are necessary to either bypass or integrate each cell. This allows to bypass less charged cells during discharging to equalise the state-of-charge (SoC) again. Additionally, defect or safety critical cells can be inactivated to be no longer under operation. While [5, 6] used relays as cell switches, [7–14] apply semiconductors like thyristors or metal-oxide-semiconductor field-effect transistors (MOSFETs). To the best advantage, relays have a galvanic isolated control voltage, which easily allows to connect any number of stages. Relays adversely do need an ongoing holding current and the physical dimensions are bigger than comparable semiconductors. Taking account of flexibility, reliability and efficiency, MOSFETs fit best for this purpose. Ertl at al. already proofed that *dynamic output voltage* are possible with switching elements on cell level. The so called "flying-battery" reduces the effort for output filters [8].

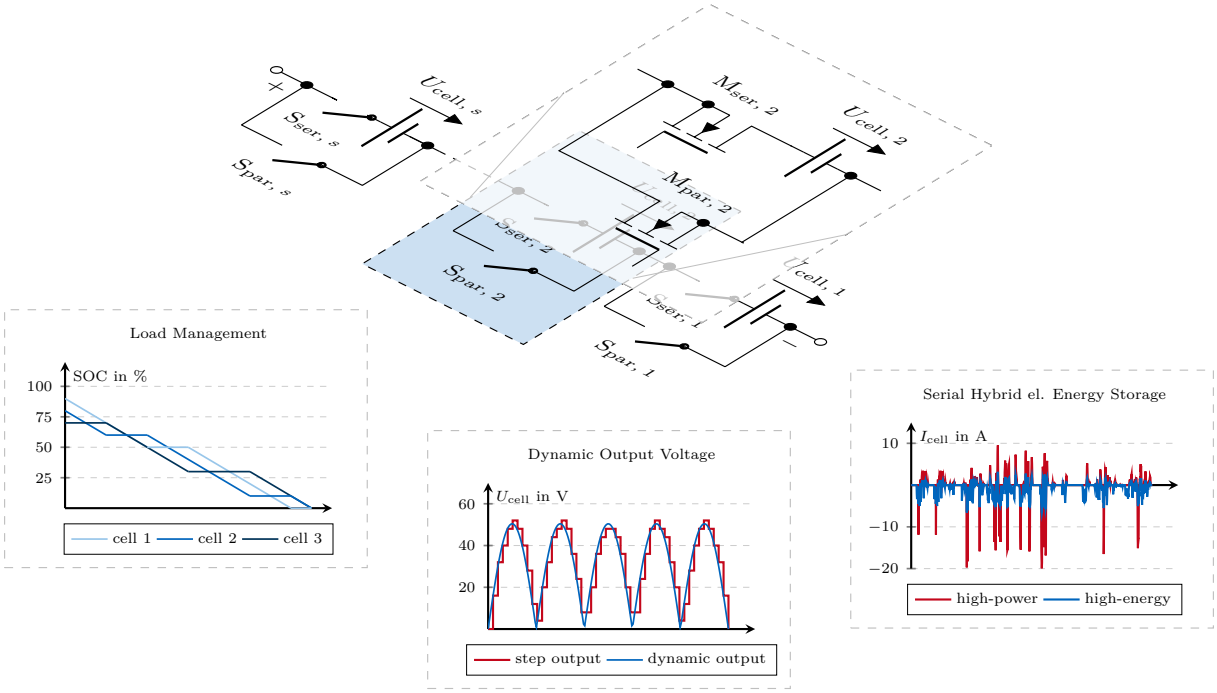


Figure 1: Battery module with switching circuits on cell level. Both switches are accomplished as MOSFETs to guarantee high reliability. This approach allows selective *load management*, a *dynamic output voltage* on stack level and *serial hybrid electrical energy storages system* (sHESS).

2 Switching Circuits on Battery Cell Level

Modularity and scalability are issues for state-of-the-art switching devices that have to be overcome. Otherwise restrictions for the algorithms exist and not every cell can be switched off in any situation. The aim is to avoid those limitations by the use of charge pumps, which can be miniaturised and integrated inside semiconductors easily [15]. Thus modularity as well as scalability is realised and load management can be implemented for each cell independently.
Reconfiguration of the serial string requires two switches for each cell. As each switch has a discrete state, in total four different switch settings are possible (cf. fig. 2). Each cell-stage represents one possible switch setting (right-to-left):

Idle state when both switches are open ($\mathbf{S_{ser,\,1}}$ and $\mathbf{S_{par,\,1}}$). This state occurs, when the whole battery system is disabled. This setting can also act as emergency stop to shut down the system automatically.

Inactive state or bypass the cell. Closing the parallel switch ($\mathbf{S_{par,\,2}}$), while keep the serial switch open ($\mathbf{S_{ser,\,2}}$), allows the stack current to flow past the cell. The input and output voltage of this cell-stage is equal, so there is no influence on stack level.

Active state or integrate the cell. Opening the parallel switch ($\mathbf{S_{par,\,3}}$) and closing the serial switch ($\mathbf{S_{ser,\,3}}$) allows the stack current to flow through the cell. The output voltage of this cell-stage increases by the belonging cell voltage ($U_{\text{cell},\,3}$).

Shorted state is strictly forbidden. Closing both switches ($\mathbf{S_{ser,\,\mathit{s}}}$ and $\mathbf{S_{par,\,\mathit{s}}}$) results in short-circuiting the cell. Not only for safety reasons but also in terms of efficiency this setting must be avoided in all circumstances.

During normal operation the states *inactive* and *active* are crucial. Those two settings allow dynamic load management and selective cell charging/discharging. As floating potentials within battery-stacks

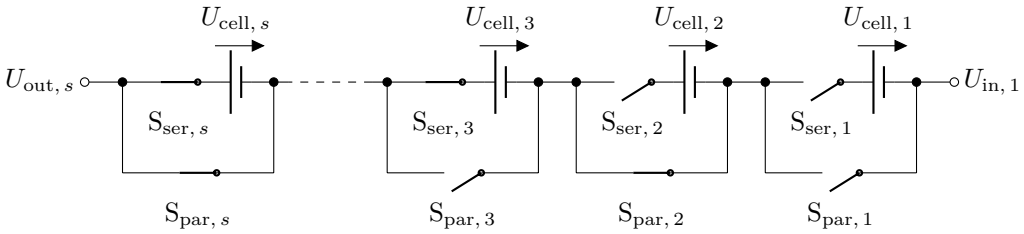


Figure 2: Cell-stages with two additional switches to achieve reconfigurability. Each stage represents one possible switch setting (right-to-left): idle state, cell bypassed, cell activated and shorted state (forbidden).

are inevitable, the potential distribution has to be studied. Therefore, the following definitions are made:

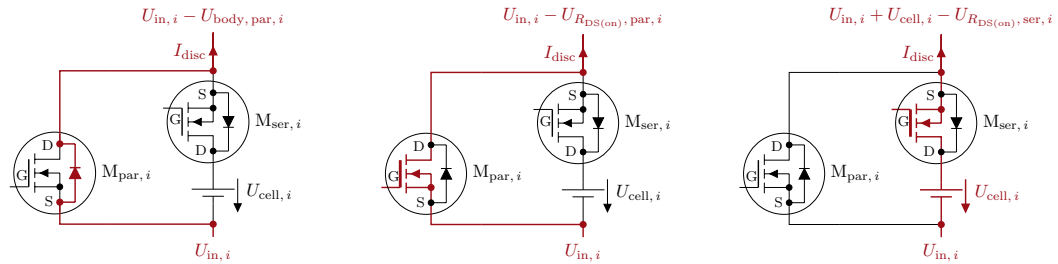
$$U_{\mathrm{in},\,1} = 0\,\mathrm{V} \tag{1}$$

$$U_{\mathrm{in},\,i} = U_{\mathrm{out},\,i-1} \tag{2}$$

$$U_{\mathrm{out},\,i} = \begin{cases} U_{\mathrm{in},\,i} & \text{inactive state, bypassed} \\ U_{\mathrm{in},\,i} + U_{\mathrm{cell},\,i} & \text{active state, integrated} \end{cases} \tag{3}$$

$$U_{\mathrm{out},\,s} = U_{\mathrm{stack}} \tag{4}$$

Due to its internal structure, the used n-channel MOSFETs have a parasitic diode facing from source to drain [16]. To avoid undesired discharging of the cells or even harmful and safety critical states, the MOSFET placement is vital (cf. fig. 3). As shown in fig. 3a during idle state the serial MOSFET ($\mathbf{M_{ser,\,i}}$) prevents the cell to discharge itself, while the parallel MOSFET ($\mathbf{M_{par,\,i}}$) allows current flowing through its parasitic diode. As the parasitic diode produces an additional voltage drop and therewith additional losses, the inactive or active state are preferred (cf. figs. 3c to 3f). Hereby the additional losses are produced by the internal on-state resistance $R_{\mathrm{DS(on)}}$ of the MOSFET.



(a) Idle state: discharge

(c) Inactive state: discharge

(e) Active state: discharge

(b) Idle state: charge

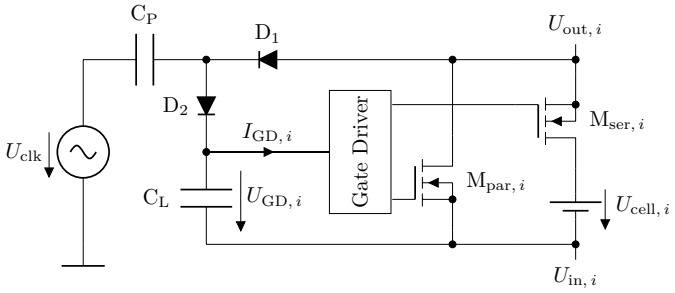
(d) Inactive state: charge

(f) Active state: charge

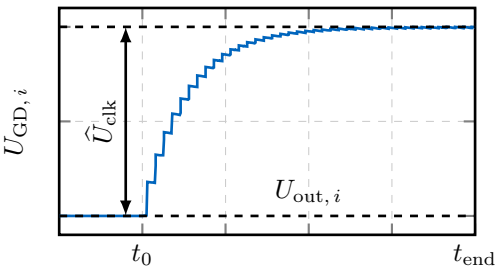
Figure 3: Possible current paths and potential levels for the different MOSFET states. In idle mode, the parasitic diode of the serial MOSFET ($\mathbf{M_{ser,\,i}}$) prevents discharging the cell. Due to lower power losses the inactive or active states are preferred.

3 Realisation of the Cell-Stages

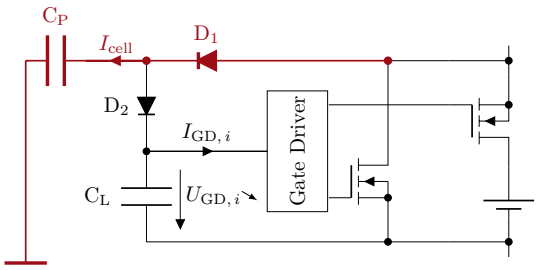
The key challenge of the hardware concept is a scalable solution to generate the gate-driver supply. [9, 13] use static voltage divider to generate the needed control voltages. In consequence of the fixed voltage ratio, the stack voltage U_{stack} must be within a limited range. Moreover, this strategy does not ensure scalability. [8] uses four MOSFETs for each stage to generate negative voltages and to implement bootstrapping to supply the gate-drivers. Therefore, continuous toggling of all MOSFETs is necessary to keep the voltage levels alive.
Basically, two methods fulfil the requirements of scalability and modularity. *Isolated DC/DC converter* are very reliable and efficient but also very cost- and space-intensive. In comparison *charge pumps* can be integrated on chip level, so they are very reasonable. Nevertheless, poor efficiency and limited current load capacity must be considered [17, 18]. Figure 4a shows a single cell-stage with its connected charge pump. While each stage needs its own gate-driver, two diodes ($\mathbf{D_1}$/$\mathbf{D_2}$) and two capacitors ($\mathbf{C_P}$/$\mathbf{C_L}$), only one clock voltage U_{clk} for all stages is necessary. The reference voltage for each charge pump is the output voltage $U_{\text{out},\,i}$ of the corresponding cell-stage. This ensures sufficient voltage levels, independent of the switch settings of stages below.
The fundamental principle is illustrated in figs. 4c and 4d. To generate the gate-driver voltage $U_{\text{GD},\,i}$, which is higher than the reference voltage $U_{\text{out},\,i}$, an additional clock voltage U_{clk} is necessary. This clock voltage generates two different states: during *OFF* state (U_{clk} = low, cf. fig. 4c) current flows from $U_{\text{out},\,i}$ through the diode $\mathbf{D_1}$ and charges the capacitor $\mathbf{C_P}$. Neglecting the voltage drop across the diode, the voltage of the capacitor $\mathbf{C_P}$ is equal to the reference voltage $U_{\text{out},\,i}$. During *ON* state (U_{clk} = high, cf. figure fig. 4d) the lower electrode of the capacitor $\mathbf{C_P}$ is shifted by U_{clk} and diode $\mathbf{D_2}$ gets conductive. Neglecting the voltage drop across the diode again, the gate-driver voltage $U_{\text{GD},\,i}$ of the capacitor $\mathbf{C_L}$ is equal to $U_{\text{GD},\,i} = U_{\text{out},\,i} + U_{\text{clk}}$. [17]



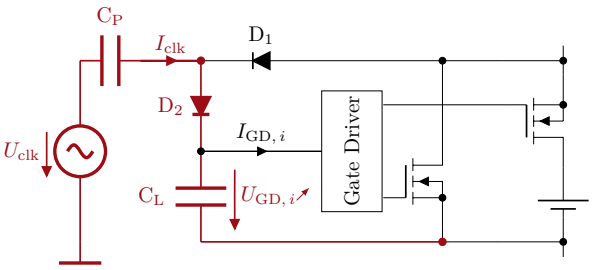
(a) Single cell-stage with its connected charge pump



(b) Gate-driver voltage U_{GD} during start-up



(c) Pump control *OFF* state



(d) Pump control *ON* state

Figure 4: Single cell-stage and its connected charge pump. For simplification the voltage drops across the diodes is neglected. The gate-driver voltage $U_{\text{GD},\,i}$ rises till steady state $U_{\text{GD},\,i} = \widehat{U}_{\text{clk}} + U_{\text{out},\,i}$ is reached (b). Both states of the pump control voltage U_{clk} are shown in (c) and (d).

The clock frequency f_{clk} as well as the capacity values C_{P} and C_{L} affect the dynamic behaviour of the charge pump and indirectly settle the maximum switching frequency f_{switch} between active or inactive state. The necessary switching frequency is also limited by the current consumption of the gate-drivers. Considering the additional forward voltage drop U_{F} of the diodes $\mathbf{D_1}$ and $\mathbf{D_2}$, the gate-driver supply voltage is calculated to [15, 19]:

$$U_{\text{GD},\,i} = U_{\text{out},\,i} + U_{\text{clk}} - 2 \cdot U_{\text{F}} - \frac{I_{\text{GD},\,i}}{f_{\text{clk}} \cdot C_{\text{P}}} \tag{5}$$

There is always a trade-off between the rise time and voltage swing evoked by the size of $\mathbf{C_L}$. For higher

clock frequencies ($f_{\mathrm{clk}} \gg 100\,\mathrm{kHz}$) it is recommended to build a multiple-stage charge pump with reduced clock voltage. Otherwise high transient voltage might produce electromagnetic interference (EMI). Those can also be reduced by limiting the rising and falling edge with an additional resistor. [19–21]

4 Experimental Results

To validate the hardware concept a laboratory prototype was developed. Figure 5 shows the switcher board with its stacked power supply and eight connected battery cells (type 18650). The power supply is fed by the activated cells. To boot up the system a tactile switch manually connects the lowest cell to the power supply input. Once the switches are activated, the stack voltage U_{stack} is used to supply the system autarchically. Large input capacitors are used as uninterruptible power supply (UPS) and do allow to inactivate all cells at the same time for a short period.

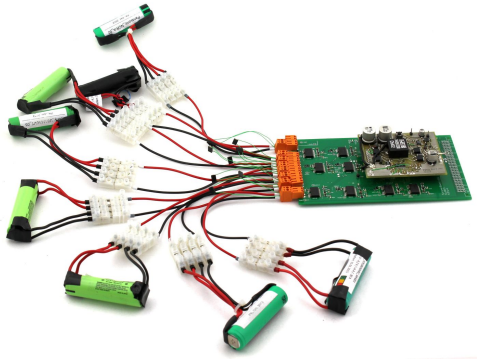
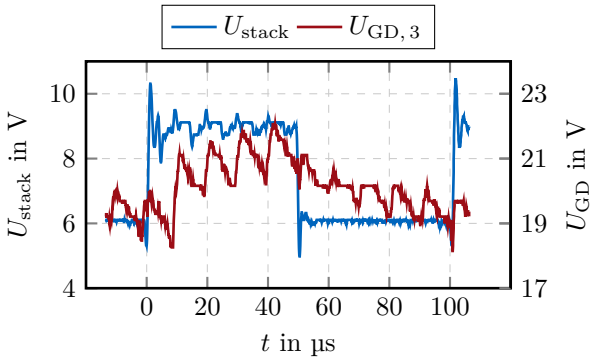


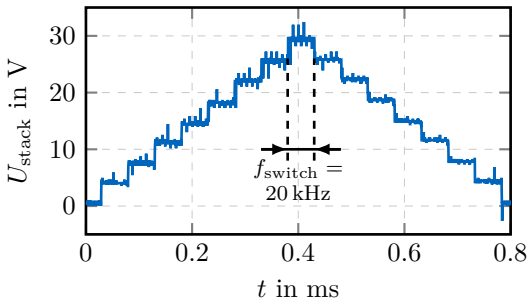
Figure 5: Laboratory prototype with eight connected battery cells (type 18650).

Figure 6a shows the stack voltage and the floating gate-driver supply voltage of the third stage (both voltages are referenced to $U_{\mathrm{in},1}$, eq. (1)). In this case, cell-stage two and three are activated while the first stage is toggled with $f_{\mathrm{switch}} = 10\,\mathrm{kHz}$. It can be seen that the charge pump is capable to follow the input voltage of the corresponding cell-stage and keeps the gate-driver supply alive. During the rising edge the additional load to charge the capacitor $\mathbf{C_{L,3}}$ is clearly recognisable in the stack voltage U_{stack} ($0\,\mu\mathrm{s} \leq t < 50\,\mu\mathrm{s}$). Inactivating the underlying cell-stage does not cause additional load and the stack voltage is quite steady ($50\,\mu\mathrm{s} \leq t < 100\,\mu\mathrm{s}$).

Figure 6b demonstrates the performance of the system. All eight cell-stages are controlled to generate a trapezoid stack voltage with a signal frequency of $f_{\mathrm{tpz}} = 1.25\,\mathrm{kHz}$. The step size which corresponds to the switching frequency of the last activated cell is $f_{\mathrm{switch}} = 20\,\mathrm{kHz}$. Nevertheless, because the switching order can be mixed, much higher signal frequencies are possible without increasing the switching frequency. The mixed order of activated cells also implies an equal load distribution on all cells. The transient behaviour generated by the fast acting MOSFETs must be analysed in detail. Especially the high dynamic behaviour influences the stack voltage. The parasitic inductive component, introduced by the copper and aluminium cell tap, is evident and limits the switching frequency. [22, 23]



(a) Stack voltage and gate-driver supply of the third stage. Cell-stage two and three are activated, first stages is toggled with 10 kHz.



(b) Trapezoid tack voltage composed of eight cell-stages. The generated signal frequency is 1.25 kHz and the switching frequency is $f_{\mathrm{switch}} = 20\,\mathrm{kHz}$.

$U_{\mathrm{clk}} = 15\,\mathrm{V}$ $f_{\mathrm{clk}} = 100\,\mathrm{kHz}$ $U_{\mathrm{F}} = 0.6\,\mathrm{V}$ $I_{\mathrm{GD}} = 6\,\mathrm{mA}$ $C_{\mathrm{P}} = 100\,\mathrm{nF}$ $C_{\mathrm{L}} = 470\,\mathrm{nF}$

Figure 6: Experimental results with the developed laboratory prototype. All corresponding charge pumps generate the floating gate-driver potentials. All eight cell-stages can be toggled with switching frequencies up to 20 kHz at any time and in mixed order.

5 Outlook on serial Hybrid Energy Storage Systems (sHESS)

As in this concept all switches are accomplished as MOSFETs a very dynamic and active *load management* is possible. Thus the utilisation of the battery pack can be maximised in every situation. As consequence of individual load management, different types of batteries or even different kinds of electrical energy storages can be interconnected to built *serial hybrid electrical energy storages system* (sHESS). This novel approach allows precisely tailored battery packs for each application to enhance performance and energy supply.
Analysing 149 standardised driving cycles comes to the conclusion, around 10 % of the total energy consumption is recuperated again with a maximum charging power of 43 % of the maximum discharge power. If this amount of energy is provided by the high power (HP) battery, the maximum power for the high energy (HE) part can be reduced to around 44 %. The approach is shown in fig. 7. All driving cycles were simulated with the same vehicle model to generate the battery power distribution, which was than normalised to its maximum level and rearranged to get the average load duration curve. Splitting this curve into the HP- and the HE-part allows cumulating the power separately to achieve not only the demandable energy but also the HP/HE-ratio.

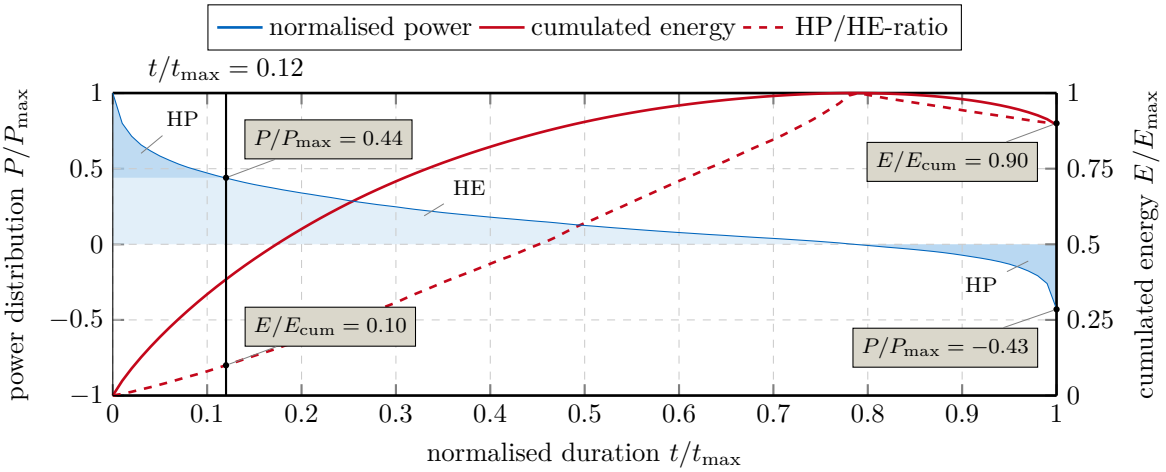


Figure 7: Analysis of 149 standardised driving cycles by normalising in power and time. Sorting the load levels in a descending order of their magnitudes generates the average load duration curve.

As an example given, one operating strategy for sHESS within EV is the maximisation of recuperated energy. Thus, a HP storage – in our case a HP lithium-ion battery – is connected when the EV decelerates. As long the HE batteries are not bypassed at the same time, the pack voltage increases while the current decreases as long as the power stays constant. This reduces the stress for HE batteries which typically increases the lifetime and duration. Because the HP-part is able to store a certain smaller amount of energy, it is activated mainly during acceleration. The recuperated energy can than be used as booster, analogue to the described behaviour while breaking.
To ensure safe operation and to implement voltage or current based algorithms on the developed laboratory prototype, an embedded measurement system for voltage and current will be integrated in the near future. Afterwards sHESS are investigated with different operating strategies which are evaluated by modelling the system.

6 Conclusion

To guarantee modularity and scalability for switching elements on cell level a convenient approach is presented in this paper. Charge pumps are used to generate floating gate-driver potentials. A first laboratory prototype does proof the concept. Eight cell-stages can be switched in mixed order without any restrictions, while the corresponding charge pumps adopt each voltage level to generate proper gate-driver potentials. The developed hardware is capable to generate *dynamic output voltages* with switching frequencies of more than 20 kHz.
The ability to influence the current path through the cell stack allows active *load management*. Each cell can be fully utilised without any expensive balancing circuits. This leads to the possibility of combining different battery types or electrical storage technologies in series without any additional power electronics. In conclusion, those *serial hybrid electrical energy storages system* (sHESS) allow tailor suited battery packs for any application regarding power and energy and simultaneously maximise the overall utilisation.

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